SEMICONDUCTOR DEVICE FOR DRIVING LIQUID CRYSTAL AND LIQUID CRYSTAL DISPLAY APPARATUS

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims benefit of priority under 35USC § 119 to Japanese Patent Application No. 2000-195940 filed on June 29, 2000 in Japan, the entire contents of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device for driving liquid crystals, that installs a memory for storing display-data such as data to be displayed and to a liquid crystal display apparatus.

Liquid crystal display apparatuses have been drawing the attention for being used as light-weight and lower-power consuming flat displays.

Shown in FIG. 5 is a block diagram of a liquid-crystal display apparatus that installs a RAM (Random Access Memory) as a display-data memory.

The liquid crystal display apparatus is provided with a liquid crystal displaying section 2, a common-electrode driver 40, a segment-electrode driver 45 and a display-data RAM 50.

The liquid crystal displaying section 2 is a simple matrix type equipped with a first transparent substrate on which common electrodes are arranged in parallel and a second transparent substrate on which segment electrodes are arranged in parallel.

The first and the second transparent substrates face each other so that the segment and common electrodes cross each other, with a liquid crystal layer interposed therebetween.

A scanning line COMi (i = 1, ..., m) is connected to each common electrode. Moreover, a signal line SEGj (j = 1, ..., n) is connected to each segment electrode.

One of the scanning lines is selected by the common-electrode driver 40 to drive a common electrode connected to the selected scanning line.

Data to be displayed stored in the display-data RAM 50 are

retrieved by the segment-electrode driver 45 and supplied to the corresponding segment electrodes via the signal lines.

The segment-electrode driver 45 and the display-data RAM 50 are fabricated on one chip, which is called a liquid crystal-driving semiconductor device.

A known liquid crystal-driving semiconductor device is shown in FIG. 6. The known device is provided with the segment-electrode driver 45 and the display-data RAM 50.

The display-data RAM 50 is provided with a cell array 51 on which RAM cells 52 are arranged in matrix, an address decoder 55, a display-data read counter/decoder 57, an I/F (interface) controller 60, a data I/O circuit 62 and an oscillator 65. Each RAM cell 52 consists of two transistors, a latch circuit having two inverter gates, and a three-state driver.

The display-data RAM 50 shown in FIG. 6 is therefore a dual-port RAM 50 in which each RAM cell 52 has ten transistors.

When a CPU (not shown) has access to the display-data RAM 50, it sends an I/F signal to the I/F controller 60. On receiving the signal, the I/F controller 60 drives the address decoder 55 and the data I/O circuit 62.

An address decided by the CPU is input to the address decoder 55 via an address bus and decoded, so that the corresponding RAM cell 52 is selected on the display-data RAM 50.

Data programming is performed such that data sent on the data bus is programmed into the selected cell on the display-data RAM 50 via the data I/O circuit 62.

Data retrieval is performed such that data is retrieved from the selected cell on the RAM 50 and sent to the data bus via the data I/O circuit 62.

Data transfer to the liquid crystal displaying section 2 is performed such that the oscillator 65 sends a clock signal to the display-data read counter/decoder 57. On receiving the clock signal, the counter/decoder 57 sends a selection signal to the RAM 50. Data is then retrieved from the corresponding RAM cell 52 and stored in the segment driver 45 in response to a latch signal output by the counter/decoder 57.

The known liquid crystal-driving semiconductor device shown in FIG. 6 has a display-data output port and a CPU-access input/output port separately, so that the CPU can have an asynchronous access to the RAM 50.

The known device however requires ten transistors for each RAM 52 because the display-data RAM is a dual-port RAM, thus becoming large in its chip size.

FIG. 7 shows another known liquid crystal-driving semiconductor device for which the chip-size problem has been solved.

The known device shown in FIG. 7 is provided with a display-data RAM 50A the same type as the display-data RAM 50 (FIG. 6) except that the RAM 50A has two transistors and two inverter gates for each RAM cell 53. The display-data RAM 50A is therefore a single-port RAM 50A. The known device in FIG. 7 is also provided with a segment-electrode driver 46.

Each memory cell 53 has six transistors, so that the chip size for the single-port RAM 50A is smaller than the known liquid crystal-driving semiconductor device shown in FIG. 6.

In the known liquid crystal-driving semiconductor device shown in FIG. 7, however, the RAM 50A has a single port that is used as a display-data output port and also as a CPU-access input/output port, so that a CPU can not have an asynchronous access to the RAM 50A.

When a CPU (not shown) tries to have access while the liquid crystal displaying section is to retrieve data from the RAM 50A, either the CPU or the displaying section has the priority whereas the other has to wait.

The liquid crystal displaying section retrieves data on a constant cycle. When the CPU has the priority, it programs data on the RAM 50A while this data has remained in the CPU-access input/output port that is the display-data output port.

This results in that, when the liquid crystal displaying section retrieves display-data from the RAM 50A, the data that has been programmed by the CPU is retrieved as the display-data. This data is different from the data to be displayed and also has no correlation with data now on display. And, if displayed,

this data causes flicker on screen, thus degrading picture quality.

On the other hand, when the liquid crystal display has the priority, the CPU takes long for data programming to the RAM 50A.

SUMMARY OF THE INVENTION

A purpose of the present invention is to provide a liquid crystal-driving semiconductor device and a liquid crystal display apparatus fabricated on a small chip on which a CPU has a quick access to memory with high picture quality.

A semiconductor device for driving liquid crystals according to the present invention includes: a single-port memory that stores display-data to be displayed on a liquid crystal displaying section; a liquid crystal driver that retrieves the display-data stored in the single-port memory on a specific cycle and sends the display-data to the liquid crystal displaying section; and a controller that controls the liquid crystal driver so that, when a CPU does not have access to the single-port memory, the display-data is retrieved from the single-port memory to the liquid crystal driver on the specific cycle and the retrieved data is sent to the liquid crystal displaying section, whereas, when the CPU has access to the single-port memory while the data is being retrieved from the single-port memory to the liquid crystal driver, a priority is given to the CPU so that the CPU starts an access operation while the liquid crystal driver stops a display-data retrieval operation, and on completion of the access operation, the liquid crystal driver starts again the display-data retrieval operation.

In the semiconductor device for driving liquid crystals according to the present invention, the controller controls the liquid crystal driver so that a priority is given to the CPU to start an access operation, and on completion of the access operation, the liquid crystal driver starts again the display-data retrieval operation.

This control operation achieves high picture quality and a quick memory access operation for the CPU.

The memory is the single-port memory and hence can be

fabricated on a small chip.

Moreover, a semiconductor device for driving liquid crystals according to the present invention includes: a single-port memory that stores display-data to be displayed on a liquid crystal displaying section; a liquid crystal driver, having a latch for storing the display-data stored in the single-port memory, that retrieves the display-data from the single-port memory on a specific cycle and sends the display-data to the liquid crystal displaying section; and a controller that generates a latch control signal and sends the latch control signal to the latch, the latch control signal being generated based on a CPU-access signal indicating an access operation of a CPU to the single-port memory and a specific signal that is synchronized with a display-data retrieval cycle for the liquid crystal driver.

Furthermore, a liquid crystal display apparatus according to the present invention is provided with the semiconductor device for driving liquid crystals and a liquid crystal displaying section.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 shows a block diagram of an embodiment of a liquid crystal display apparatus according to the present invention;

FIG. 2 shows a circuit diagram of a latch of a segment-electrode driver of the liquid crystal display apparatus;

FIG. 3A shows a circuit diagram of an asynchronous-access controller of the liquid crystal display apparatus;

FIG. 3B shows a circuit diagram of an R-S flip-flop of the asynchronous-access controller shown in FIG. 3A;

FIG. 4 shows a timing chart for indicating an operation of the asynchronous-access controller;

FIG. 5 shows a block diagram of a matrix liquid crystal display apparatus;

FIG. 6 shows a block diagram of a known liquid crystal-driving semiconductor device; and

FIG. 7 shows a block diagram of another known liquid

crystal-driving semiconductor device.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Embodiments according to the present invention will be disclosed with reference to FIGS. 1 to 4.

FIG. 1 shows a block diagram of an embodiment of a liquid crystal display apparatus according to the present invention.

The liquid crystal display apparatus is provided with a liquid crystal displaying section 2 and a liquid crystal-driving semiconductor device. The semiconductor device includes a segment-electrode driver (also called a liquid crystal driver) 10, an asynchronous-access controller 20 and a display-data RAM 50B for storing data to be displayed (display-data), etc.

The display-data RAM 50B is provided with a cell array 51A on which RAM cells 53 are arranged in matrix, an address decoder 55, an inverter gate 56, a display-data read counter/decoder 57, an I/F (interface) controller 60, a data I/O circuit 62 and an oscillator 65. The display-data RAM 50B is a single-port RAM in which each RAM cell 53 consists of two transistors and a latch circuit having two inverter gates.

The liquid crystal displaying section 2 is configured such that a first transparent substrate on which common electrodes are arranged in parallel and a second transparent substrate on which segment electrodes are arranged in parallel face each other so that the segment and common electrodes cross each other, with a liquid crystal layer interposed therebetween.

A scanning line is connected to each common electrode. A signal line is connected between each segment electrode and the corresponding output terminal of the segment-electrode driver 10.

One of the scanning lines is selected by a common-electrode driver like the one shown in FIG. 5 to drive a common electrode.

The segment-electrode driver 10 is provided with a sensing circuit 12, latch circuits 14 and 16, and a driver 18 for each signal line.

The sensing circuit 12 senses data retrieved from the corresponding RAM cell 53. The latch circuit 14 stores the output

of the sensing circuit 12 in response to a latch signal S_{L2} sent from the asynchronous-access controller 20. The latch circuit 16 stores the output of the latch 14 in response to an inverted signal of a latch signal S_{L1} sent from the display-data read counter/decoder 57. The driver 18 sends the output of the latch circuit 16 to the corresponding signal line.

The latch circuits 14 and 16 consist of two clocked-inverter gates and one inverter gate each, as shown in FIG. 2. Supplied to clock terminals of the clocked-inverter gates are a latch signal S_{L1} and its inverted signal, respectively.

The asynchronous-access controller 20 generates the latch signal S_{L2} based on a CPU-access signal sent from the I/F controller 60 and the latch signal S_{L1} sent from the display-data read counter/decoder 57.

Disclosed next is an operation of the preferred embodiment according to the present invention.

When a CPU (not shown) has access to the display-data RAM 50B, it sends an I/F signal to the I/F controller 60. On receiving the signal, the I/F controller 60 activates the address decoder 55 and the data I/O circuit 62 and sends the CPU-access signal to the asynchronous-access controller 20. The CPU-access signal is also sent to the display-data read counter/decoder 57 via the inverter gate 56 to deactivate the counter/decoder 57.

An address decided by the CPU is input to the address decoder 55 via an address bus and decoded, so that the corresponding RAM cell 53 is selected on the display-data RAM 50B.

Data programming is performed such that data sent on the data bus is programmed into the selected RAM cell 53 on the display-data RAM 50B via the data I/O circuit 62.

Data retrieval is performed such that data is retrieved from the selected RAM cell 53 on the RAM 50B and sent to the data bus via the data I/O circuit 62.

When the CPU has no access to the display-data RAM 50B, in other words, data is sent to the liquid crystal displaying section 2 from the RAM 50B, the display-data read counter/decoder 57 is in an active state because no CPU-access signal is generated

by the I/F controller 60.

On receiving a clock signal sent from the oscillator 65, the counter/decoder 57 sends a selection signal to the RAM 50B. Data is then retrieved from the corresponding RAM cell 53 and sent to the segment-electrode driver 10. The data retrieval is performed on a specific cycle by the driver 10.

The data retrieved and sent to the segment-electrode driver 10 is sensed by the sensing circuit 12 and stored in the latch circuit 14 in response to a latch signal S_{L2} from the asynchronous-access controller 20.

The output of the latch circuit 14 is further stored in the latch circuit 16 in response to an inverted signal of a latch signal S_{L1} the display-data read counter/decoder 57. The output of the latch circuit 16 is sent to the corresponding signal line via the driver 18 and displayed on the liquid crystal displaying section 2.

Disclosed next is the asynchronous-access controller 20 before disclosure of, in what timing, the latch signal S_{L2} is output by the controller 20.

FIG. 3A shows a circuit block diagram of the asynchronous-access controller 20 used in the liquid crystal display apparatus.

The asynchronous-access controller 20 shown in FIG. 3A is provided with inverter gates 21, 23, 25 and 29, 3-input NOR gates 22, 24 and 28, a delay circuit 26 and R-S flip-flops 27 and 30.

The latch signal S_{L1} is sent to the input terminal of the inverter gate 21 and also the reset terminal of the R-S flip-flop 30. The output of the inverter gate 21 is sent to one of the three input terminals of each of the NOR gates 22 and 24. The output of the NOR gate 22 is sent to the set terminal of the R-S flip-flop 27 via the inverter gate 23.

The CPU-access signal is sent to either of the remaining two input terminals of each of the NOR gates 22 and 24 and also one of the three input terminals of the NOR gate 28.

The output of the NOR gate 24 is sent to the reset terminal of the R-S flip-flop 27. The flip-flop 27 outputs the latch signal S_{L2} which is further sent to the input terminal of the delay circuit

26 and either of the remaining two input terminals of the NOR gate 28.

The output of the delay circuit 26 is sent to the remaining one terminal of the NOR gate 24 and also the remaining one terminal of the NOR 28 via the inverter gate 25.

The output of the NOR gate 28 is sent to the set terminal of the R-S flip-flop 30 via the inverter gate 29. The output of the flip-flop 30 is sent to the remaining one terminal of the NOR gate 22.

Each of the R-S flip-flops 27 and 30 is provided with two NAND gates and one inverter gate, as shown in FIG. 3B.

Disclosed next with reference to FIG. 4 is that, in what timing, the latch signal S_{L2} is output by the asynchronous-access controller 20.

a) In timing T1, or when the CPU has no access to the display-data RAM 50B while the latch signal S_{L1} is at "H" (a high level), the asynchronous-access controller 20 outputs a pulse signal for a period corresponding to a delay time of the delay circuit 26 as the latch signal S_{L2} in synchronism with the rising moment of the latch signal S_{L1}. Data retrieved from a cell of the RAM 50B is stored in the latch circuit 14 via the sensing circuit 12. The delay time is decided according to a period of time required for data retrieval from a RAM cell 53.

The output of the latch circuit 14 is then stored in the latch circuit 16 when the latch signal S_{L1} output by the display-data read counter/decoder 57 falls to "L" (a low level) in synchronism with a data-retrieval operation of the segment-electrode driver 10.

b) In timing T2, or when the latch signal S_{L1} is raised to "H" while the CPU is having access to the RAM 50B, since the CPU has a priority for access, the asynchronous-access controller 20 outputs a pulse signal as the latch signal S_{L2} for a period corresponding to a delay time of the delay circuit 26 on completion of the access operation. Data retrieved from a RAM cell 53 is stored in the latch circuit 14 via the sensing circuit 12 in response to the latch signal S_{L2}. This data is further stored in the latch 16 when the latch signal S_{L1} falls to "L".

c) In timing T3, when the CPU starts an access operation even though the latch signal S_{L2} has been output in synchronism with the rising moment of the latch signal S_{L1}, the CPU has a priority, so that a data-latch operation is halted. On completion of accessing by the CPU, a pulse signal, or the latch signal S_{L2} is output again for a period corresponding to a delay time for the delay circuit 26. Data retrieved from a RAM cell 53 is stored in the latch circuit 14 via the sensing circuit 12 in response to this latch signal S_{L2}. This data is further stored in the latch circuit 16 when the latch signal S_{L1} falls to "L".

d) In timing T4, when the CPU starts an access operation while no data-latch operation has been performed, the access operation is only performed by the CPU whereas no latch signal S_{L2} is output.

e) In timing T5, after the sequential operations in b), when the CPU starts again an access operation while the latch signal S_{L1} is "H", the access operation is only performed with no latch signal S_{L2} being output, even though it is the correct data-latch timing. This is because that a data-latch operation has already been successfully performed in b).

As disclosed above, according to the preferred embodiment, a single-port RAM is used as the built-in display-data RAM 50B. When the CPU starts an access operation while the liquid crystal displaying section 2 is retrieving display-data from the display-data RAM 50B, the CPU has a priority for the access operation. Then, on completion of the access operation, the display-data is retrieved again from the display-data RAM 50B and sent to the liquid crystal displaying section 2 (timing T3).

The present invention offers a small chip size and high picture quality. Moreover, a quick access operation is achieved by giving a priority to the CPU.

Display-data output by a RAM cell 53 is once stored in the latch circuit 14 in response to the latch signal S_{L2} and then stored in the latch circuit 16 at the inverted signal of the latch signal S_{L1}. Display-data is thus always output to the liquid crystal displaying section 2 in synchronism with the falling edge of the latch signal S_{L1}. In other words, the output to the displaying

section 2 is not dependent on data-latch timing by the latch signal S_{L2} and hence a display on the liquid crystal display will not be affected by the data-latch timing.

A pulse width for the CPU-access signal wider than ((a pulse width for the latch signal S_{L1})- (a delay time for the delay circuit)) do not allow the use of the asynchronous-access controller according to the preferred embodiment. This will, however, cause any particular problem because a pulse width for the CPU-access signal is usually much narrower than that for the latch signal S_{L1}.

The liquid crystal displaying section 2 may be of active matrix type instead of simple matrix type.

Moreover, DRAM (Dynamic Random Access Memory) can be used as the display-data RAM instead of SRAM (Static Random Access Memory) used in the preferred embodiment. Not only that, any other types of memory having memory cells aligned in a scanning direction from which display-data can be retrieved at once can be used instead of the display-data RAM.

As disclosed, the present invention offers a small chip size and high picture quality, and also achieves a quick memory access operation for CPU.